## ET3034TUx - 4.3 - Design rules of crystalline silicon

Let's discuss the operating principle of the crystalline silicon solar cell.

In this block we will discuss several technical aspects which play an important role in the collection of the light excited charge carriers and the reduction of the optical losses.

Let's look at the solar cell.

In week 2, we have discussed how an illuminated p-n junction can operate as a solar cell.

In the illustrations we have used in week 2, both the p-doped and n-doped region have the same thickness.

If we look at the c-Si technology, this is not the case in real devices.

Let's look at the most conventional crystalline silicon solar cell.

The solar cell is based on a p-type silicon wafer.

The n-layer, in this illustration colored yellow, is the n-doped layer in the crystalline silicon PV technology.

This layer is often called the emitter layer.

This n-type emitter layer is much thinner than the wafer, the emitter has a thickness in the order of 1 micron.

The rest p-doped wafer can be in the order of 100 up to 300 microns.

As discussed in week 3, a large fraction of light is absorbed close to the front surface of the solar cell.

This is the generation profile as we have discussed in week 3.

You see that in the first 10 microns most charge carriers are excited.

By making the front emitter layer very thin, a large fraction of the light excited charge carriers generated by the incoming light are created within the diffusion length of the p-n junction.

One of the processing methods to make the emitter layer is by solid state diffusion.

The wafers are placed in a furnace, where the dopant atoms are present in atmosphere in the form of phosphine.

These atoms react at these high temperatures with the surface.

At these high temperatures the dopant atoms are mobile in the solid and based on Fick's law the dopant atoms will diffuse into the wafer.

Similar as we have discussed in week 2 for charge carrier diffusion, net diffusion occurs when there is a density gradient.

The diffusion process is controlled such that the dopants penetrate into the solid to establish the desired emitter thickness.

Now we are going to look at how the charge carriers in crystalline silicon solar cells are collected.

We will discuss the crucial issues which play an important role in this charge collection: this includes the emitter layer, the metal contacts and the back contact.

Let's start with the emitter layer: At the p-n junction the light excited minority charge carriers are separated at the p-n junction.

The minority electrons in the p-layer drift to the n-layer.

These electrons have to be collected.

Since the silicon n-emitter is not conductive enough we have to use the more conductive metal contacts.

The metal contacts are placed on top of the emitter layer.

Here the metal contacts are made of the cheap metal aluminum.

This means that the electrons have to diffuse laterally through the emitter layer to the contact to be collected.

Let's see what the challenges for this transport of electrons to the contacts are .

First, last week we have discussed the importance of the high lifetimes of charge carriers.

High lifetime guarantees large open-circuit voltages, or in other words the best utilization of the band gap energy.

This means that we have to reduce the recombination losses as much as possible.

In addition recombination limits the collected current as well.

Recombination in silicon occurs as discussed earlier through Shockley-Read-Hall recombination and Auger recombination.

Let's consider Shockley-Read-Hall recombination.

A bare c-Si surface contains many defects.

The surface silicon atoms have some valence electrons which cannot make a molecular orbital with the absent neighboring atoms.

These valence orbitals containing only one electron at the surface act like defects, also called dangling bonds.

At these defects the charge carriers can recombine through the SRH process.

The probability and speed at which charge carriers can recombine is usually expressed in terms of the surface recombination velocity.

Since a large fraction of the charge carriers are generated close to the front surface, a high surface recombination velocity at the emitter front surface will lead to charge carriers losses and consequently lower short-circuit current densities as well.

For example, high-quality monocrystalline silicon wafers have no defect rich grain boundaries in the bulk.

The lifetime of the charge carriers is limited by the recombination processes at the wafer surface.

In order to reduce the surface recombination, two approaches are used.

The first is based on reducing the number of defects at the surface.

This can be achieved by the deposition of a thin layer of a different material on top of the surface.

This material partially restores the bonding environment of the silicon atoms.

In addition, the material must be an insulator, it must force the electrons to remain in and move through the emitter layer.

Typical chemical passivation layers being used on emitter layers are silicon oxide and silicon nitride.

Silicon oxide layers are formed by heating up the silicon surface in an oxygen-rich atmosphere.

The surface oxidizes resulting in a thin layer of silicon oxide.

SiN can be deposited using plasma-enhanced chemical vapor deposition.

We will come back to that process technology when we talk about thin-film PV technologies.

A second approach to reduce the surface recombination velocity is to reduce the minority charge carrier density near the surface.

As the surface recombination velocity is limited by the minority charge carriers, a low as possible minority charge carrier density at the surface region would be beneficial.

It means that with increasing the doping of the emitter layer, we decrease the density of the minority charge carriers.

This results in a lower recombination velocity at the surface.

However, this is again in competition with the diffusion length of the minority charge carriers.

In this case the hole is indicated by the blue dot.

Note, that many charge carriers are generated by the blue-ish photons close to the surface.

To utilize these light excited minority charge carriers, the diffusion length of the holes has to be large enough to reach the depletion zone at the p-n junctions as indicated by the blue arrow.

Increasing doping levels, decreases the diffusion length of the minority holes in the emitter layer.

Here you see an example in which the diffusion length has become so small that the minority charge carriers are unable to reach the p-n junction.

Therefore, too high doping levels or too thick emitter layers would result in a poor blue response or in other words low EQE values in the blue part of the solar spectrum.

Such layer could be referred to as a "dead layer" as the light excited minority charge carriers can not be collected.

Now, we look in more detail to the metal-emitter interface.

A problem at this metal-emitter interface is that we cannot use an insulating passivation layer, like SiOx or SiN anymore as we need electrons to conduct from the semiconductor to the metal.

This means that the metal-semiconductor interface has more defects and therefore an unwelcome high interface recombination velocity.

In addition a metal-semiconductor material induces a barrier for the majority charge carriers.

In view of the scope of this course, it is too much detail to discuss this barrier in great detail.

Keep in mind that this high barrier will give rise to a higher contact resistance.

Again high doping levels can reduce the recombination velocity at the metal-semiconductor interface and reduce the contact resistance.

As a consequence it is preferred to reduce the area of the interface between the metal and the semiconductor to minimize the recombination at the interface defects as much as possible, and to have the emitter directly under the contact as heavily doped as possible.

This higher doped region in is indicated by N++.

In the figure you see that the contact area between metal and interface is kept as small as possible.

The sides of the metal contacts are buried in the insulating passivation layer.

The area below the contact has been heavily doped.

These two approaches reduce the recombination and collection losses at the metal contact.

The classic metal grid pattern on top of a solar cell looks like this.

It is the road map for the electrons.

Indicated in red, we see the highway for the electrons in the middle of the top surface of the solar cell.

These are called the busbars.

The smaller country roads going from the busbar to the edge of the solar cell, are called 'fingers'.

First, the fingers have a resistance R.

If L is the length of the finger, W the width of the finger and H is the height of the finger, and rho is the electrical resistivity of the metal, we can describe the resistance R as rho times length divided by the height and the width.

The equation shows that the longer the path length for an electron will be, the larger the resistance the electron experiences.

In addition, the smaller the cross-section (width times height) of the finger, the larger the resistance will be.

Note, that the resistance of the contacts will act as a series resistance in the equivalent electric circuit.

Larger series resistance will result in lower fill factors of the solar cell as discussed in week 3.

This means that you would like to have the finger cross-section as large as possible.

In this figure we see that the electrons in the emitter have to travel in the lateral direction to arrive at the contact.

Since the n-type silicon has a higher resistivity as the metal, the charge carriers in the emitter layer also experience a resistance.

In one of the exercises in this week it is demonstrated that the power loss due to the resistivity of the emitter layer, scales with the finger spacing to the power 3.

As the metal contacts are at the front surface, they act as an unwelcome shading object, or in other words light incident on the front contact area cannot be absorbed in the PV active layers.

So you would like to keep the contact area as small as possible, which is in competition with the fact that you would like to have a large as possible cross-section.

So basically you would like to have a small as possible width and a high as possible height to comply with these requirements as demonstrated by the left contact.

As you see we have several effects, which are in competition.

Let's look for a moment at the relation between losses and the finger spacing.

With increasing finger spacing the power losses of the solar cell decreases due to shading.

In contrast, the losses due to the resistivity in the emitter layer and the metal fingers increases.

This means that the total loss has a minimum.

Similar plots can be made for the width of the contact.

The larger the width, the larger the losses due to shading.

The resistive losses in the metal fingers decrease with increasing finger width.

Again there exists a width, which has a minimum loss.

Optimizing the front contact pattern is therefore a complex interplay between the finger width and spacing.

At the back surface of the solar cell we have similar issues playing a role.

As the electrons have to be collected in the n-type layer, the holes are collected at the back contact.

As electrons are the only charge carriers that exist in the metal, you have to realize that the holes recombine with the electrons at the contact interface.

If the distance between the p-n interface and the back contact is smaller than the typical diffusion length of the minority electrons, the latter mentioned minority electrons can be lost at the defects at the back contact interface due to the SRH recombination.

How can we reduce this loss mechanism?

First, we can reduce again the area between the metal contact and the semiconductor.

We can make point contacts.

The rest of the rear surface is then passivated by an insulating passivation layer, similar as we have discussed for the cases of the emitter front surface.

The loss mechanism of recombination of electrons at the back contact can be further reduced by a so-called back surface field.

A higher p-doped region is placed above the point contacts at the rear surface, indicated by P++.

How does the back surface field work?

For the moment we have put the solar cell on its side.

Below the solar cell you see the band diagram indicating the various interfaces.

The interface between the lower-doped p-region and the higher-doped p-region acts like a p-n junction.

In this case it will act as a barrier for the light excited minority electrons in the lower-doped region to diffuse to the back surface.

The space charge field behaves like a passivation of the defects at the back contact interface and allows to have higher levels for the electron minority density in the p-doped bulk.

Up to now we have talked about managing the charge carriers.

Now we are going to discuss the management of the photons in a crystalline silicon solar cell device.

The optical loss mechanisms are shading, reflection losses, parasitic absorption losses in the non-PV active layers and light that is not absorbed in the silicon layers and is lost at the back contact.

Shading losses are caused by the front contact grid as discussed earlier.

The optimum contact grid at the front is a competition between reduction of the shading losses and a reduction of the resistivity losses in the metal contact and the emitter layer.

Secondly, the reflection at the front surface can be considered as a loss mechanism.

Last week we have discussed two approaches to reduce the losses.

The first one was based on the Rayleigh film principle.

By putting a film with a refractive index smaller than that of silicon wafer between air and the wafer, you can reduce the losses.

The optimum value for the refractive index of the intermediate layer equals the square root of the product of refractive indices of the two other media.

For silicon and air at 500 nm this leads to an optimum refractive index of 2.1.

Note, that in practice a solar cell is encapsulated under a glass plate.

The glass plate will be beneficial to refractive index grading as well, reducing the reflection losses further.

Secondly, using the concept of destructive interference we can choose the thickness and refractive index of an anti-reflection coating such that in a certain wavelength the irradiance coupled out of solar cell is minimized.

The light reflected from the front surface is in anti-phase with the light reflected from the back surface, as discussed last week.

The thickness of such layer should be the wavelength divided by the 4 times the refractive index.

If we take a welcome reflective index of 2.1 we arrive for light of 500 nm at an optimal thickness of 60 nm for an anti-reflection based on destructive interference.

As we have discussed earlier, one of the typical passivation layers of standard crystalline silicon is silicon nitride.

Here we see a multicrystalline silicon wafer without the SiNx layer.

We see that a lot of light is reflected by the wafer.

Next to it, we see a multicrystalline silicon with a silicon nitride passivation layer.

As you can see much less light is being reflected.

Interestingly, the refractive index of SiN is in the range of 2 up to 2.2 at 500 nm, close to the optimum for refractive index grading.

Typical thicknesses are in the same range as the 60 nm discussed earlier.

Note, that the surface of the solar cell looks a bit blue-ish.

This shows that the reflection of blue light by the SiNx is larger than for the other wavelengths.

As discussed last week, texturing of the surface can improve the light incoupling as well.

Light that is reflected at the textured surface, can be reflected at angles in which the trajectory of the light ray is incident somewhere else on the surface.

Here the light can be still coupled into the silicon.

Secondly, the scattering at textured surfaces will couple the light under angles into the wafer.

This means that the absorption path length will be enhanced.

This certainly enhances the welcome absorption of the light with a wavelength above 900 nm.

The texture on the wafers can be realized with wet-etching approaches.

Here you can use an interesting property of the 100 surface.

This anisotropic etching can be used when etching a crystalline silicon wafer with an initial 100 surface orientation.

Etching of such wafer leads to textured surfaces with pyramid structures having only 111 oriented surfaces.

In this picture you can see such textured surface of a monocrystalline silicon wafer as processed at the DIMES lab in Delft.

Using such etching procedures it is even possible to have a silicon wafer looking black, as shown here in the second picture.

Here we see a flat multicrystalline silicon layer with and without silicon nitride.

Under these wafers, we see two wafers with and without silicon nitride layers, as well.

The only difference is that the two wafers at the bottom have textured surfaces.

The wafers are placed in the same illumination conditions as the flat wafers.

By eye you can already see that these surfaces are darker and therefore reflect less light.

So, we have discussed the general design rules for crystalline silicon solar cells.

In the next block I will show you three different concepts of high-efficiency crystalline silicon solar cells.

As you will see, they are based on the design rules we have discussed in this block.

See you in the next block!